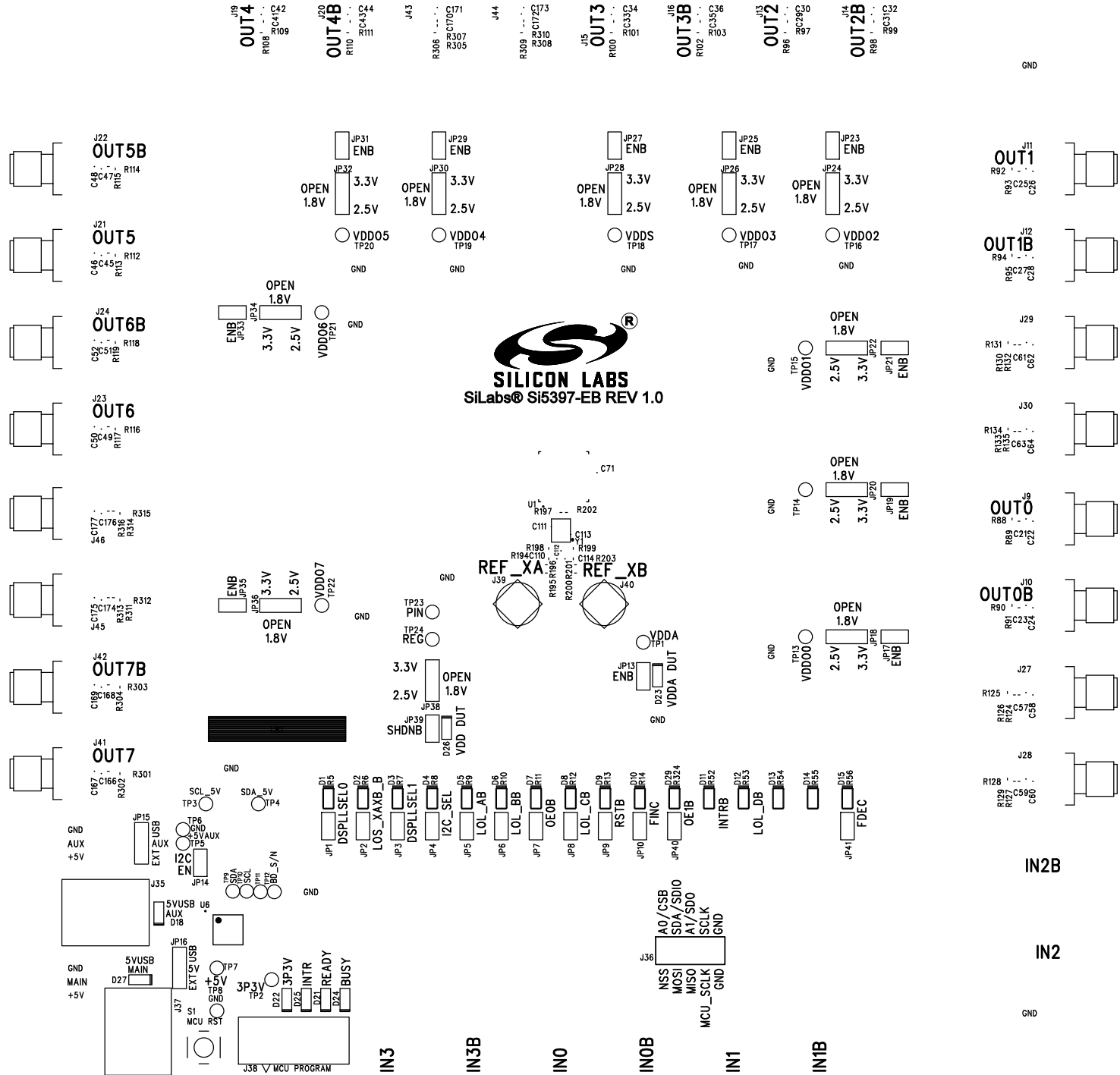
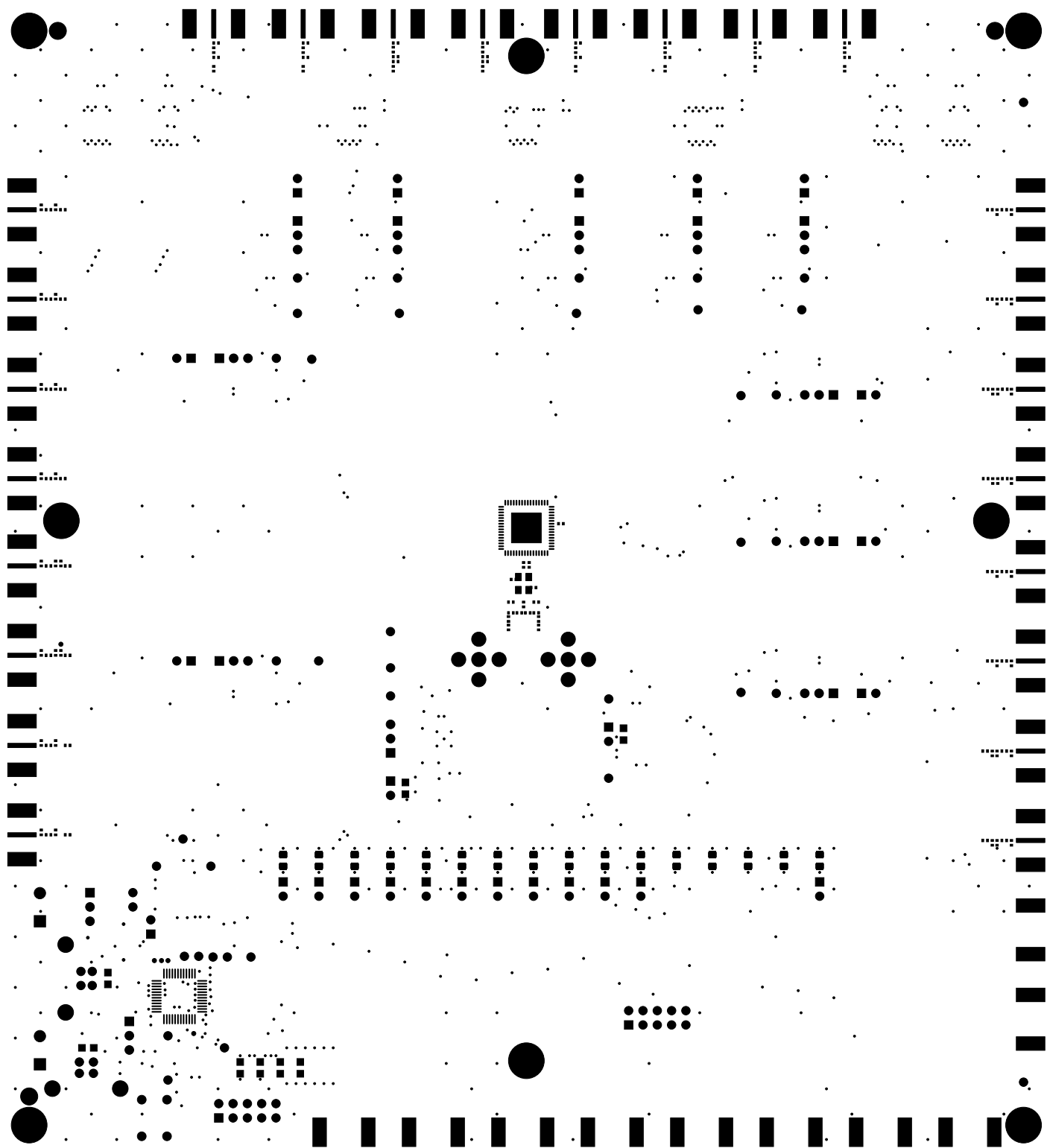


PRIMARY SILKSCREEN

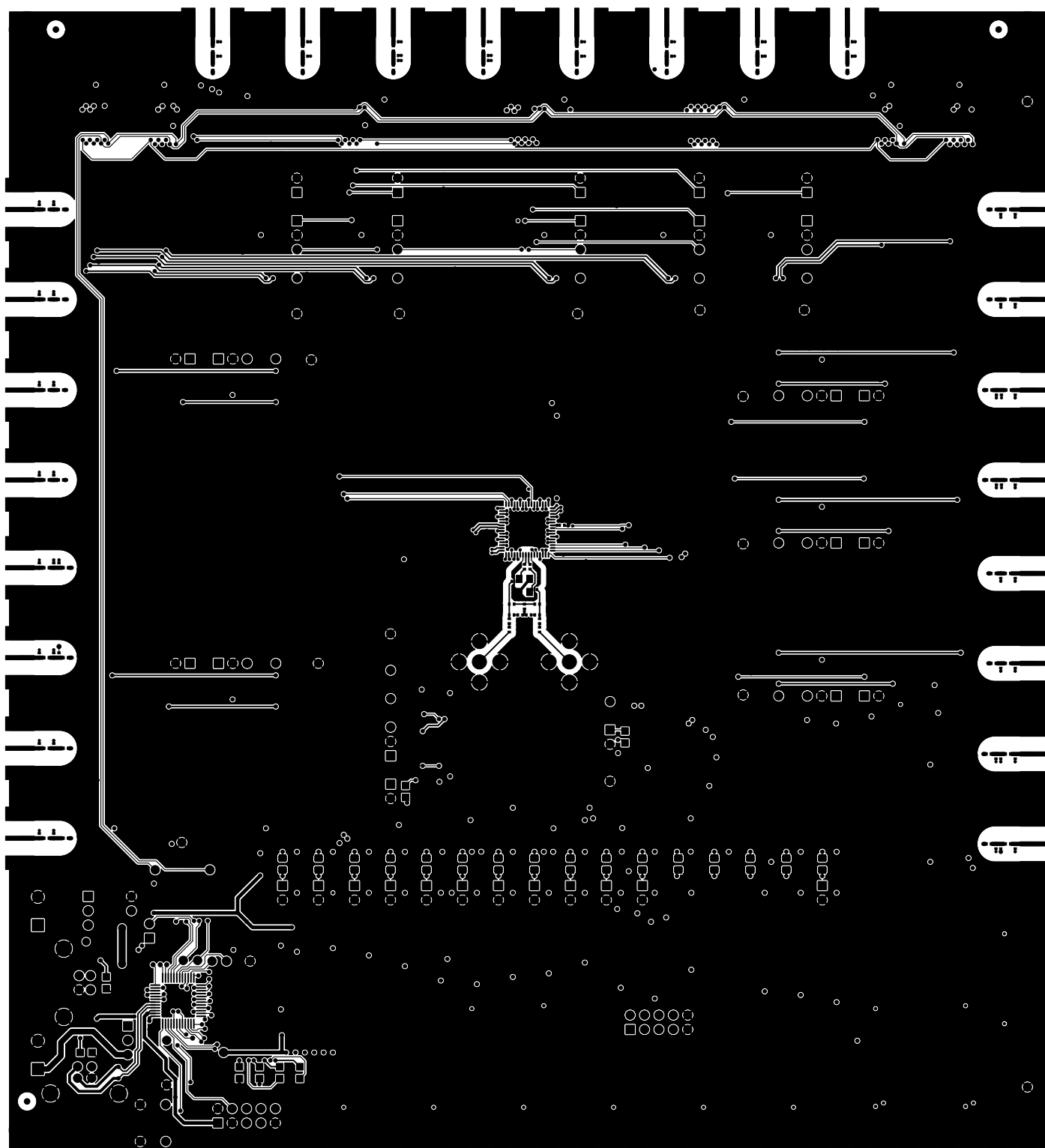




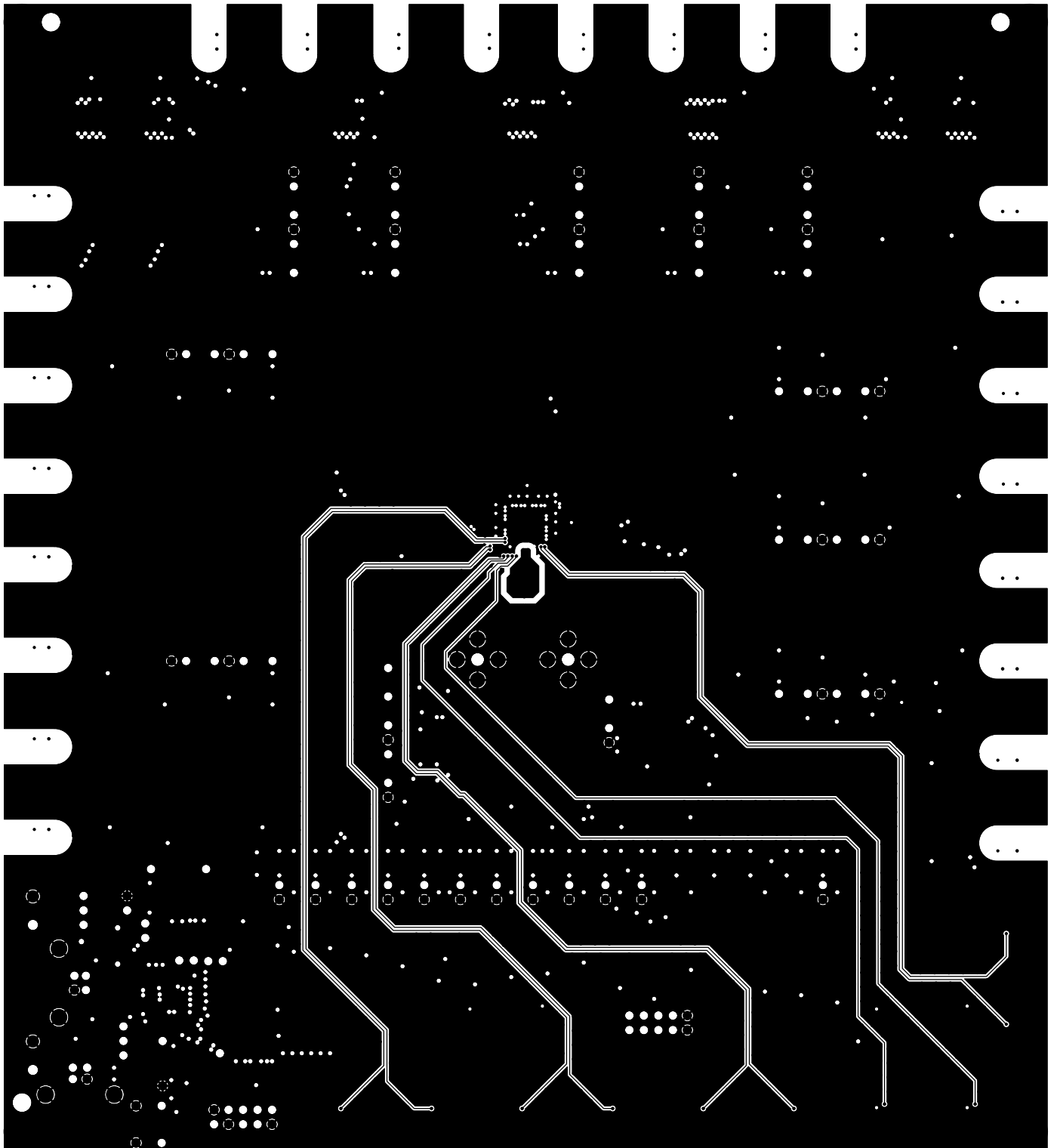
PRIMARY SOLDER MASK



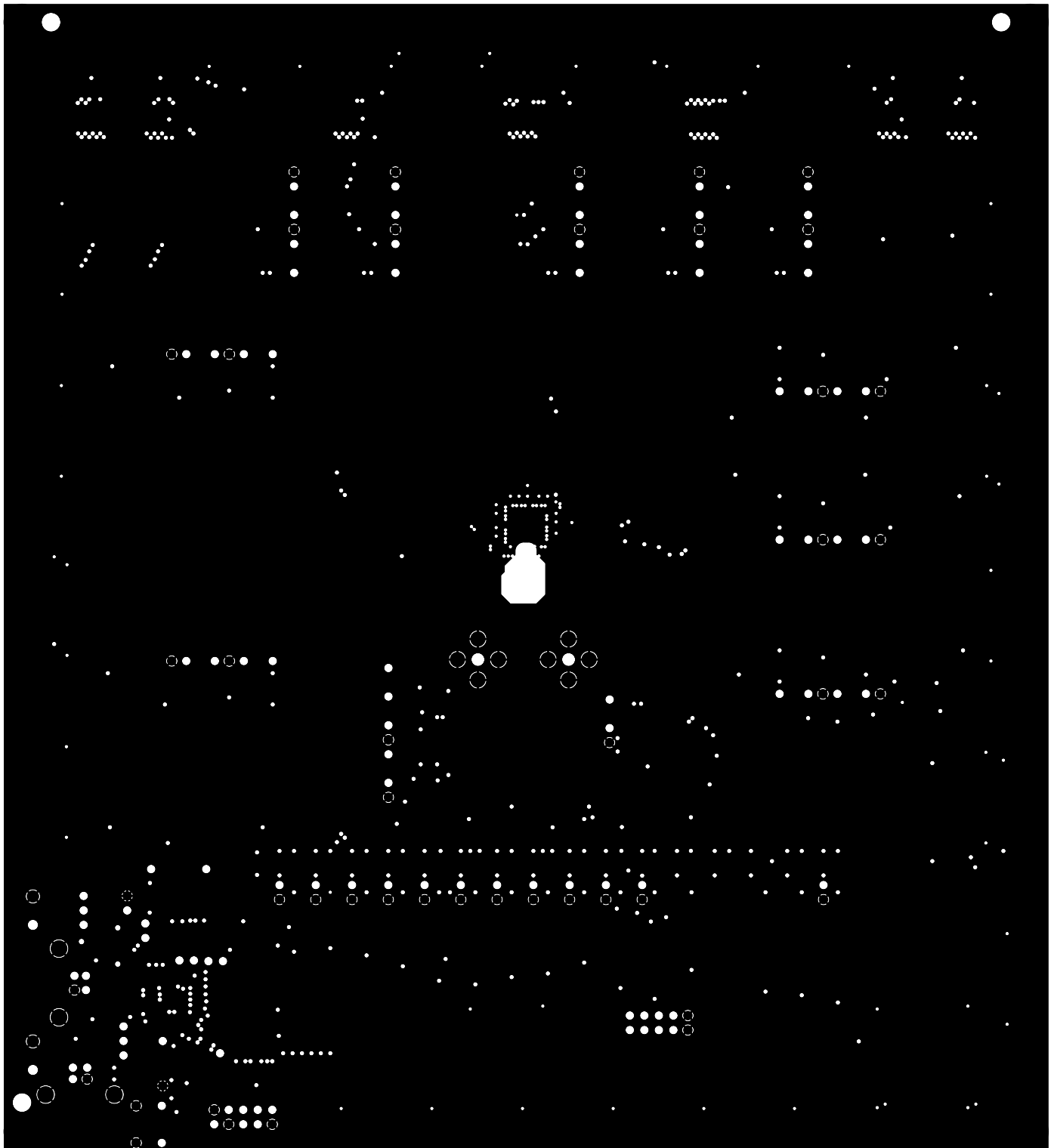
PRIMARY SIDE



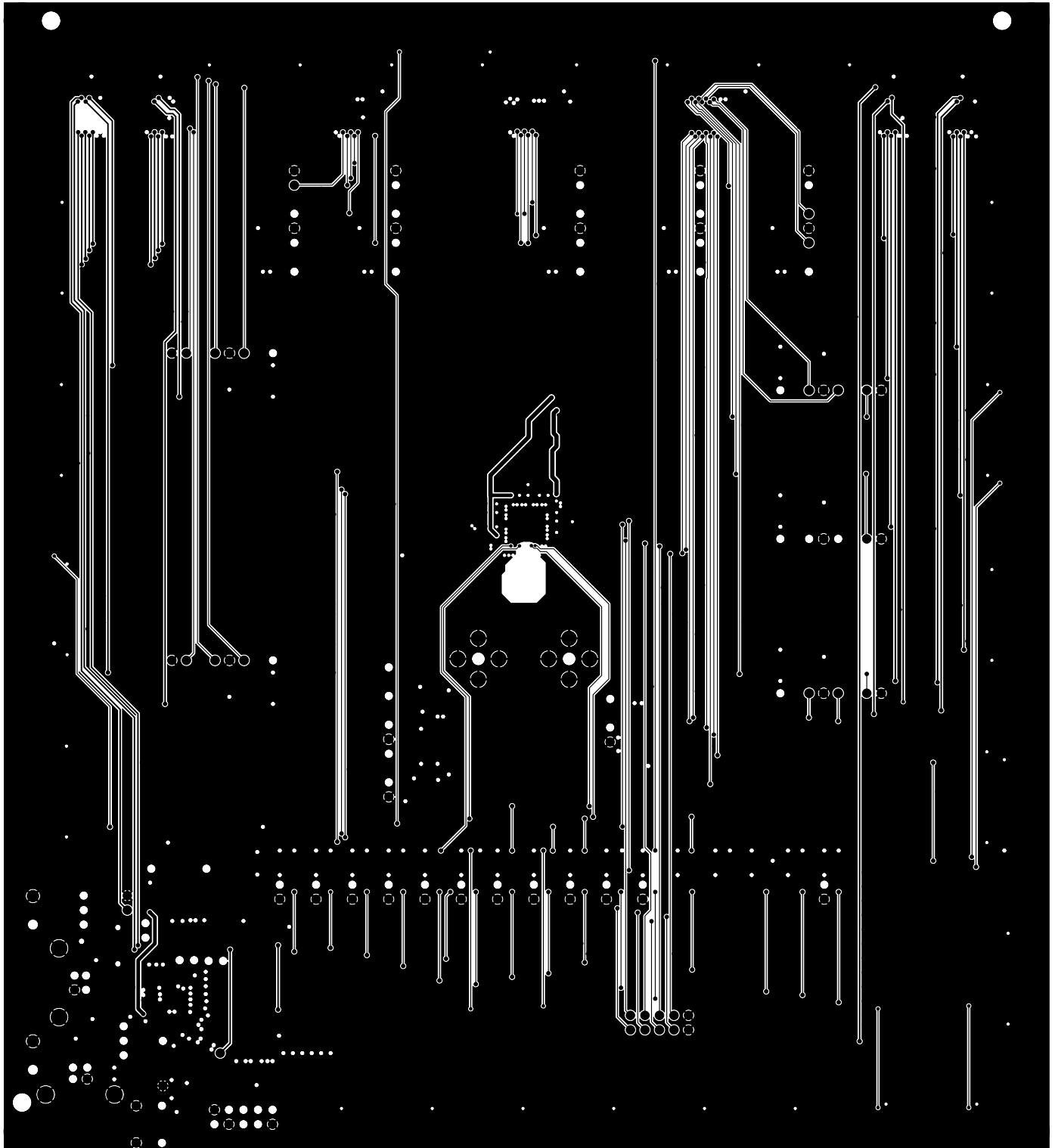
LAYER 02



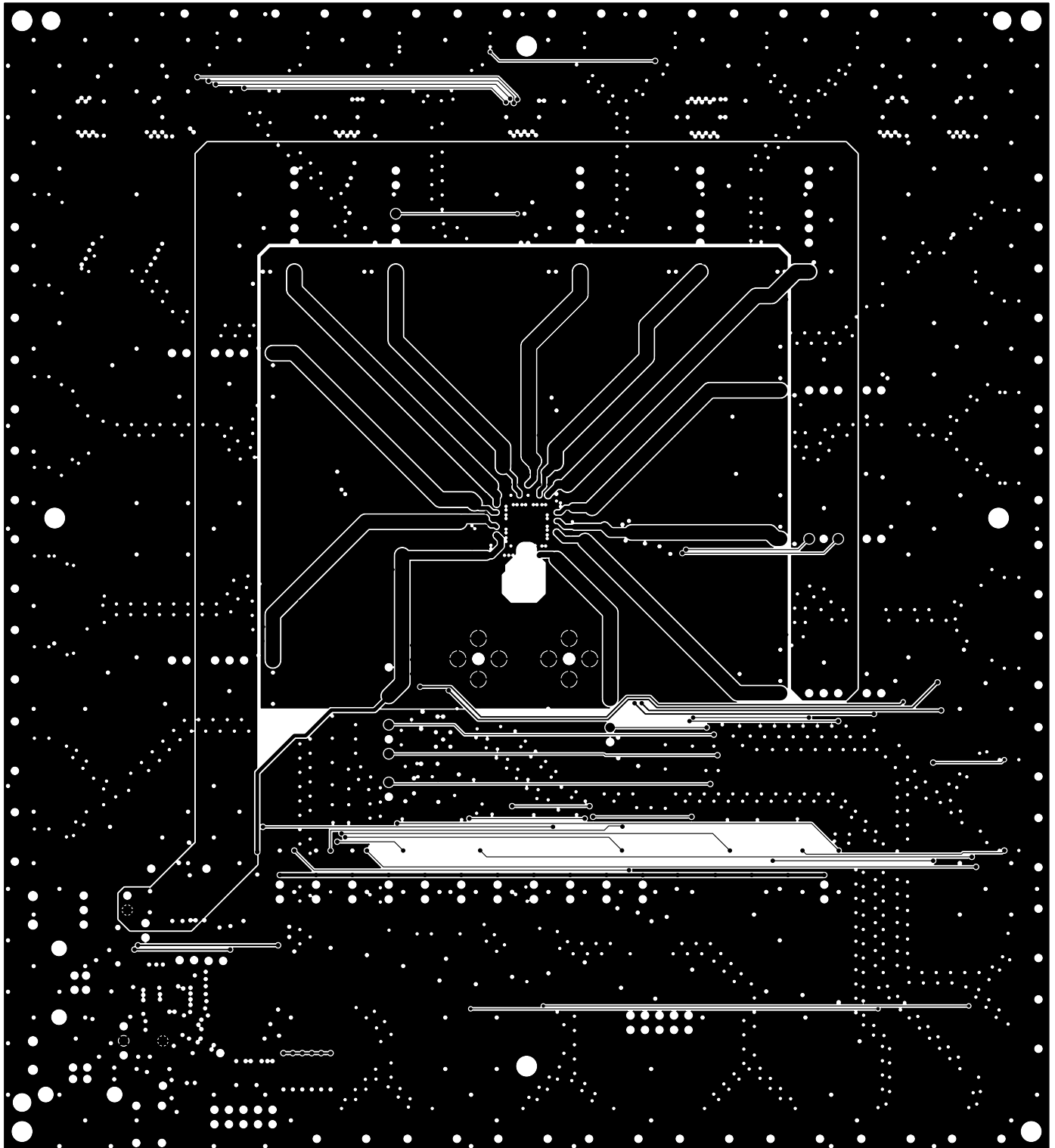
LAYER 03



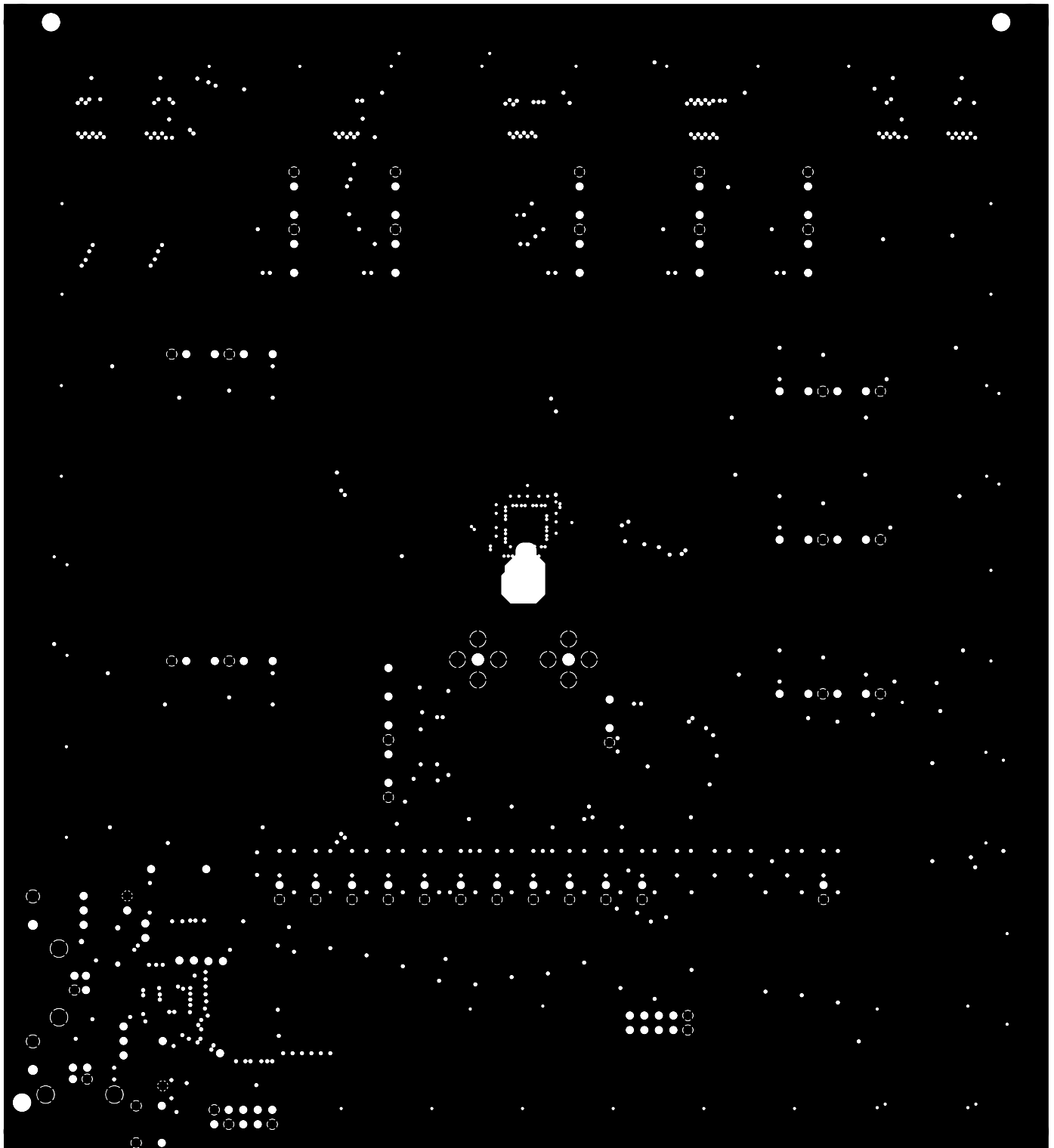
LAYER 04



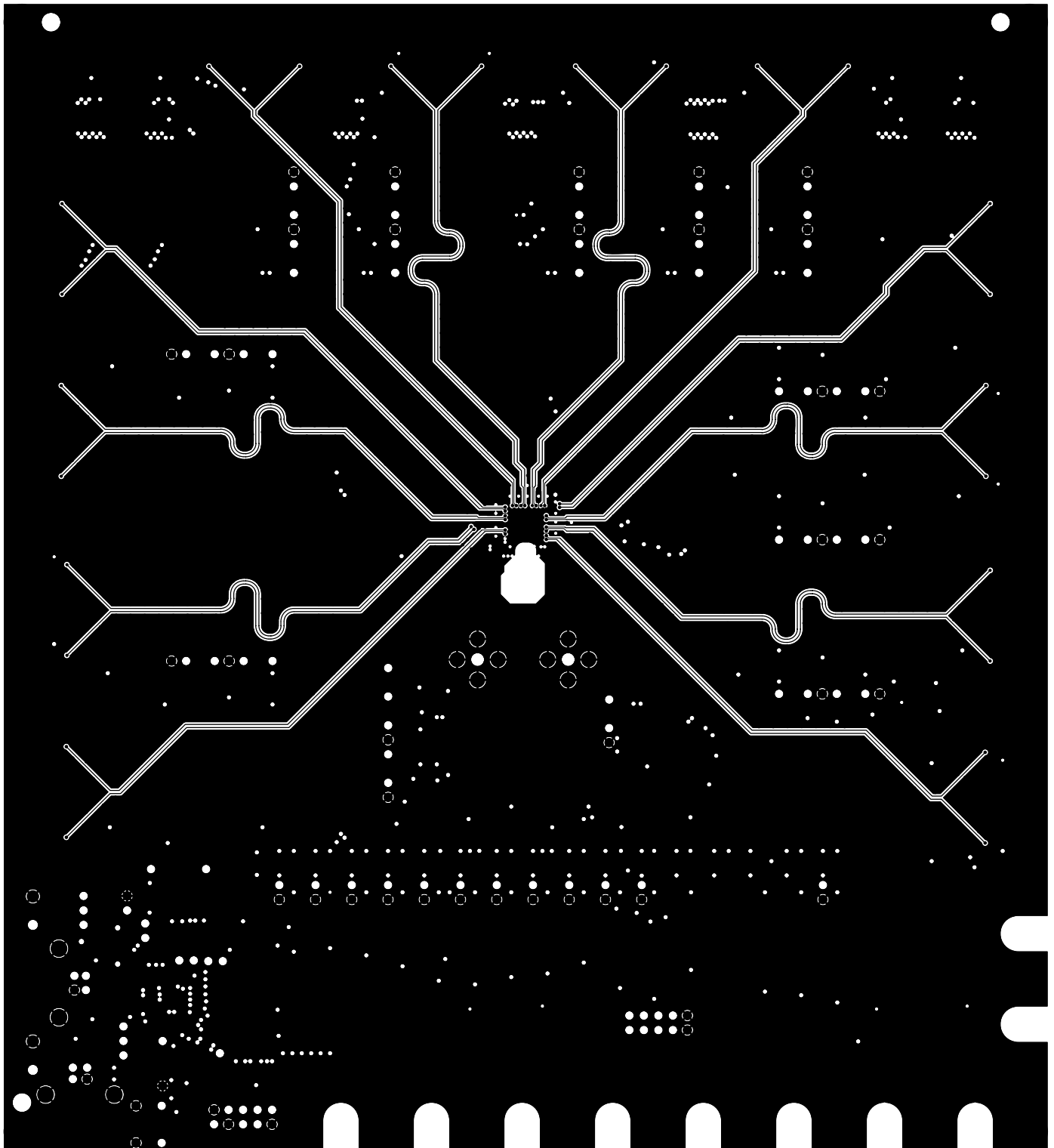
LAYER 05



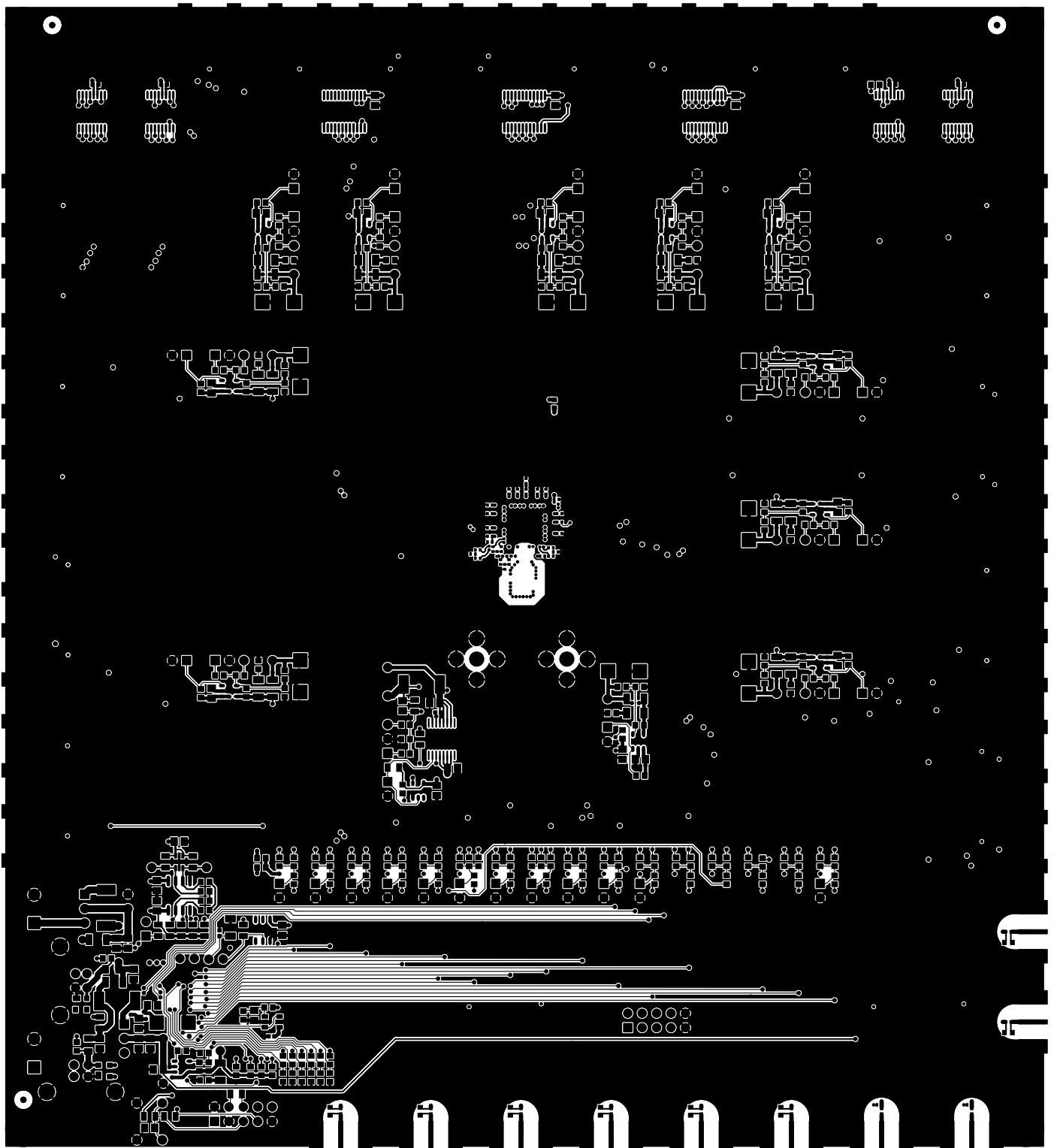
LAYER 06



LAYER 07

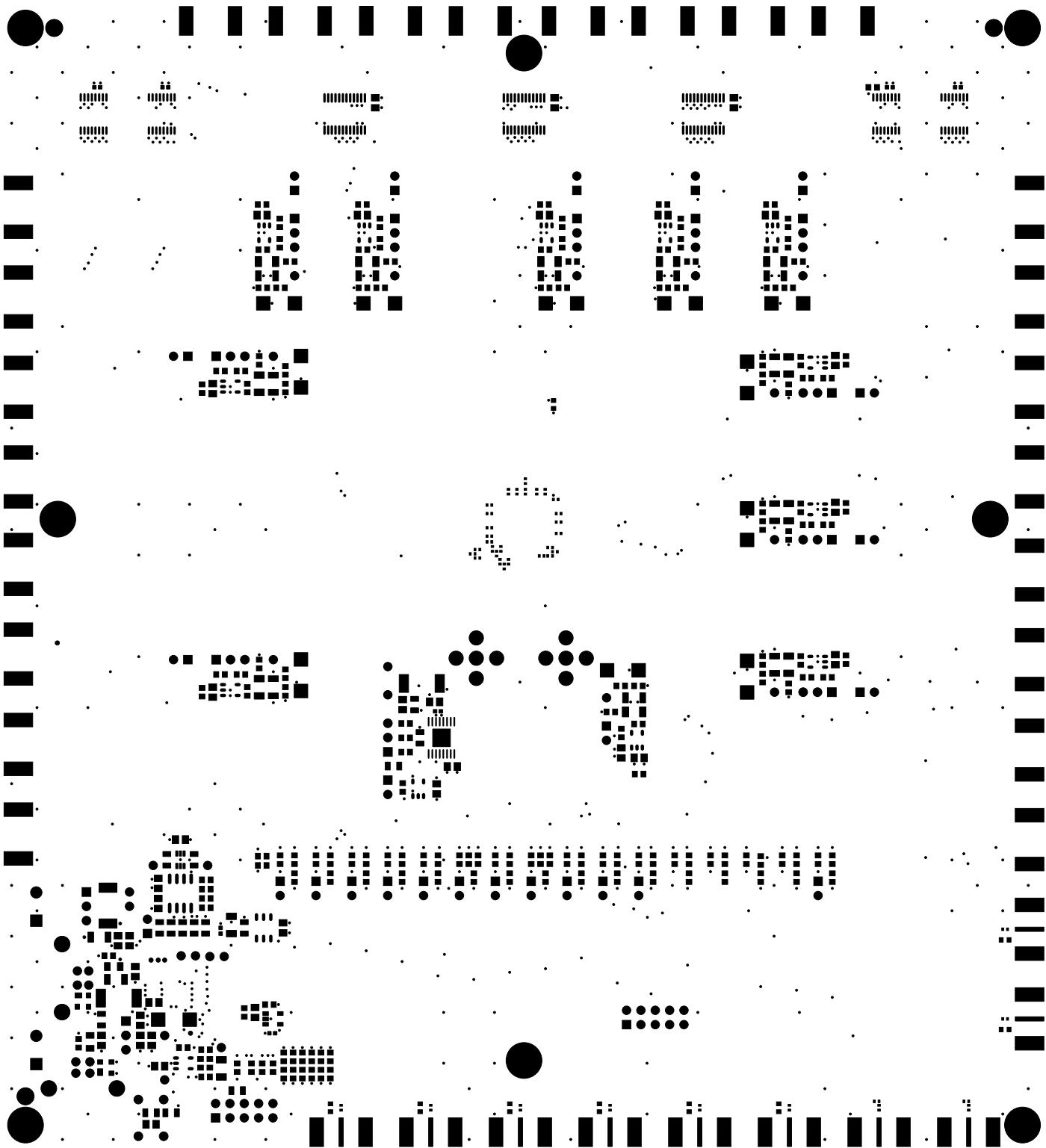


SECONDARY SIDE



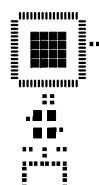


SECONDARY SOLDER MASK



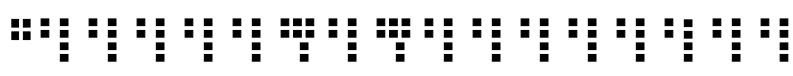
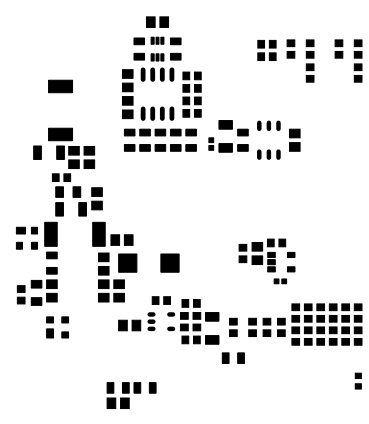
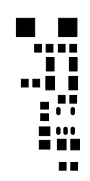
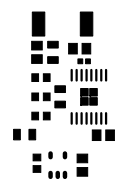
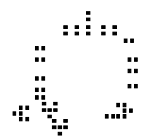
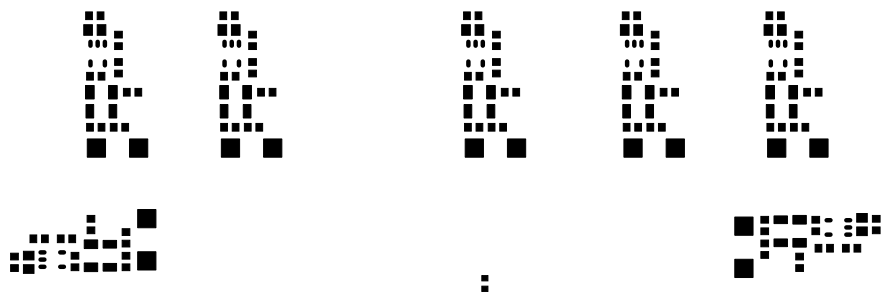
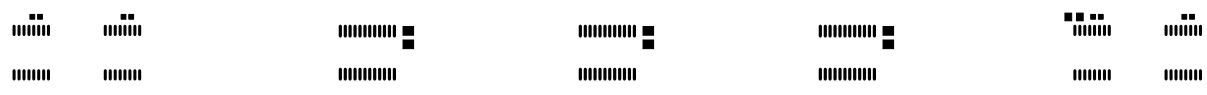


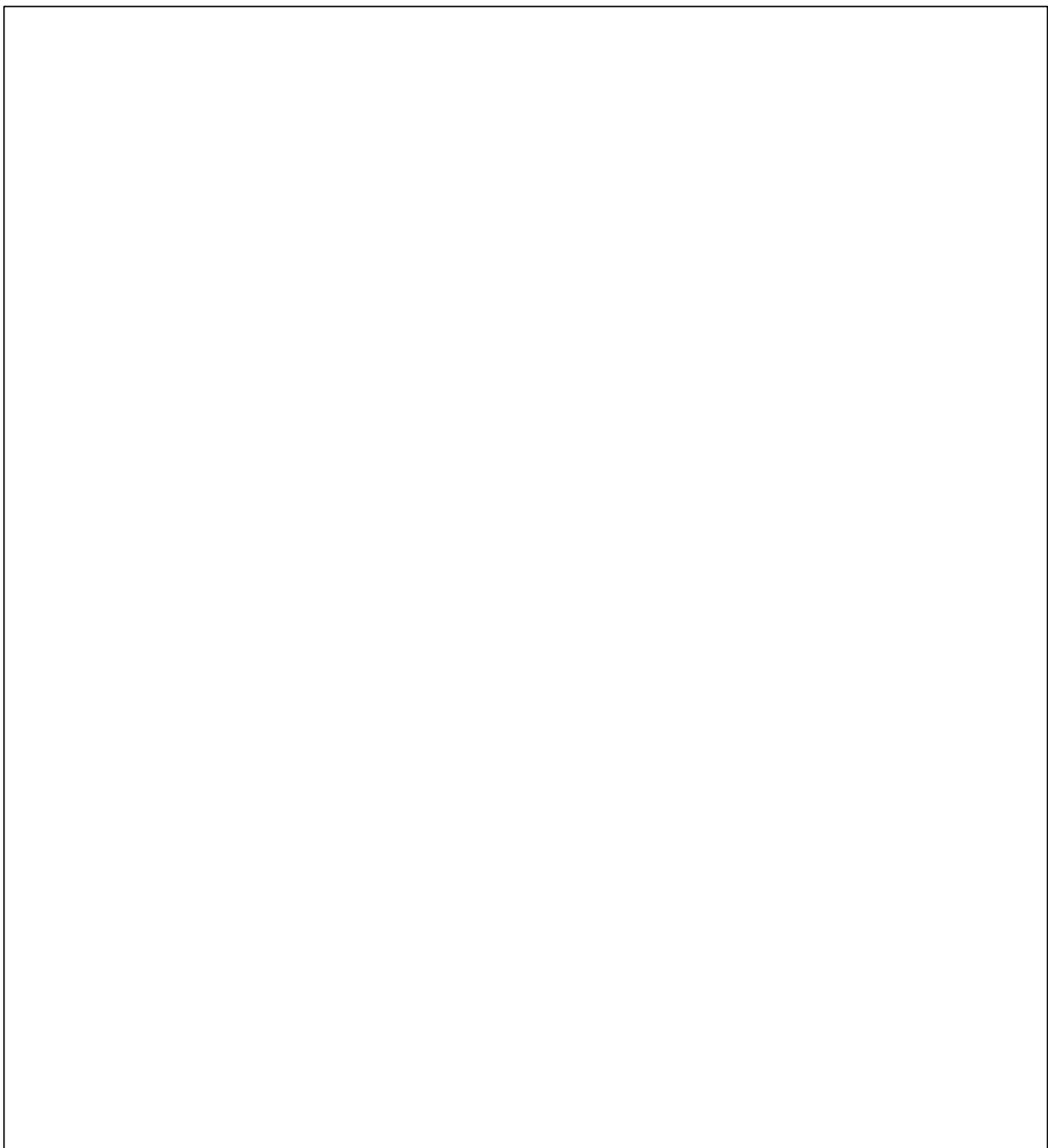
PRIMARY SOLDER PASTE

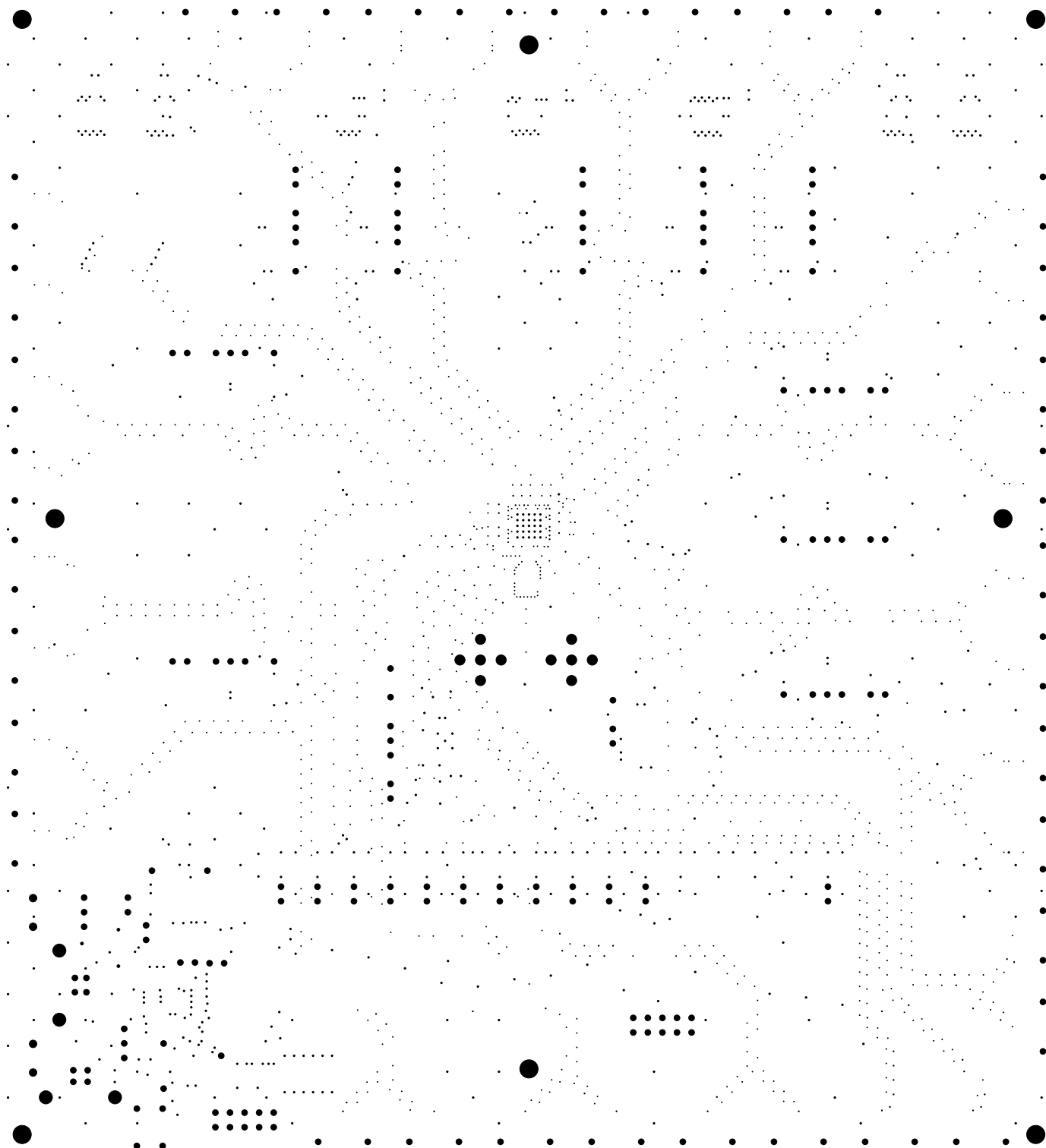




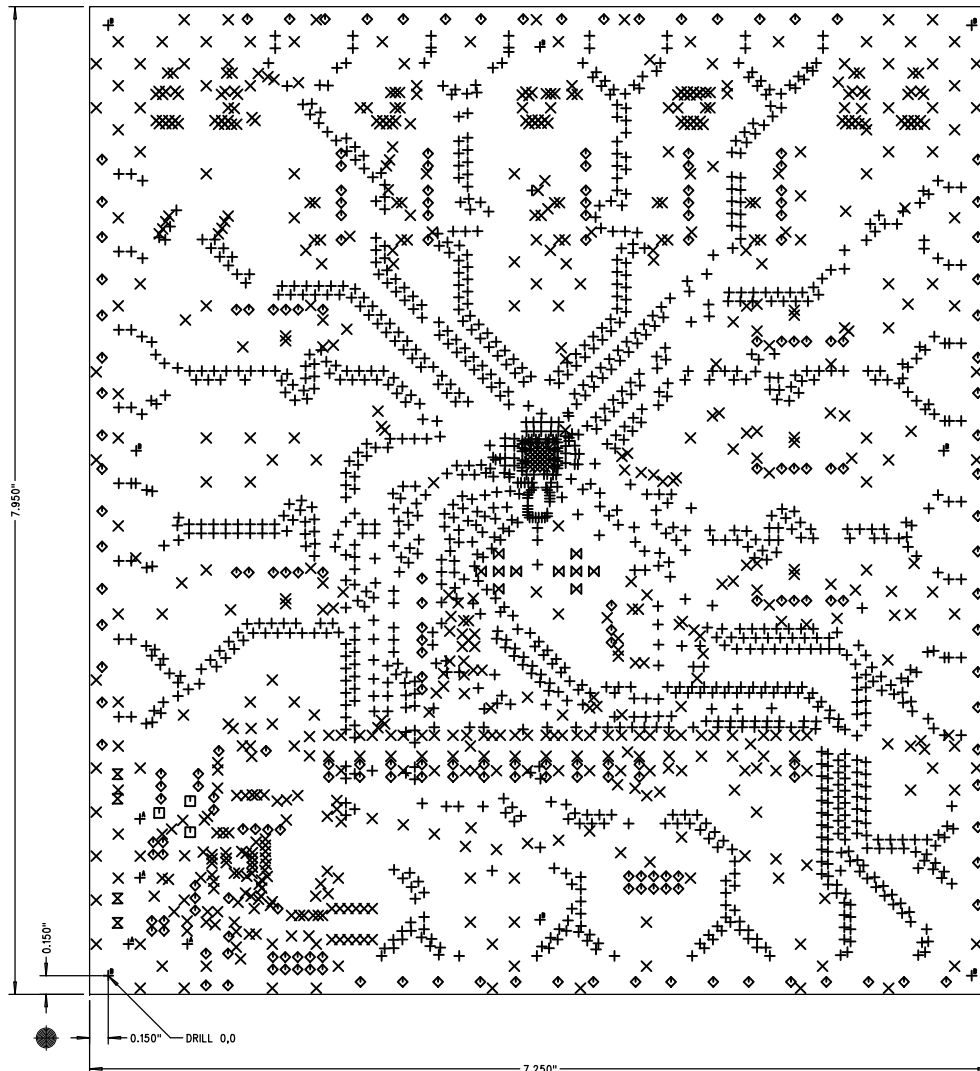
SECONDARY SOLDER PASTE







PRIMARY DRILL



NOTES : UNLESS OTHERWISE SPECIFIED

1. MANUFACTURE IN ACCORDANCE WITH IPC-6012, TYPE 3, CLASS 2.
2. END PRODUCT FEATURES SHALL NOT VARY MORE THAN 20% FROM ARTWORK ORIGINALS.
3. LAMINATE AND PREPREG SHALL BE AS PER IPC-4101/26,83,98 WITH A DECOMPOSITION TEMPERATURE $\geq 345^{\circ}\text{C}$, COLOR, NATURAL.
4. COPPER WEIGHT SHALL BE 0.5 OZ./SQ. FT. BEFORE PLATING.
5. ALL PLATED THROUGH HOLES SHALL HAVE A MINIMUM OF 0.001" COPPER.
6. DRILL HOLE TOLERANCE AFTER PLATING SHALL BE ± 0.003 ".
7. MINIMUM ANNUAL RING SHALL BE 0.001".
8. MINIMUM ANNUAL RING AT EMERGENT CONDUCTORS SHALL BE 0.003".
9. FINAL PCB THICKNESS SHALL BE 0.062" $\pm 10\%$.
10. WARP/TWIST SHALL NOT EXCEED 1.0%.
11. FINISH SHALL BE LPI, BLUE SMOBC, ENIG BOTH SIDES.
12. SILKSCREEN WITH NONCONDUCTIVE WHITE EPOXY INK.
13. INTERNAL 0.175MM TRACES TO BE 50 OHM $Z_0 \pm 5\%$.
EXTERNAL 0.275MM TRACES TO BE 50 OHM $Z_0 \pm 5\%$.
TOP 0.762MM TRACES TO BE 50 OHM $Z_0 \pm 5\%$ REF TO L03.
BOTTOM 0.762MM TRACES TO BE 50 OHM $Z_0 \pm 5\%$ REF TO L06.
14. VENDOR TO PROVIDE PCB MICRO-SECTION OF COUPON AREA & TDR TEST REPORT.
15. REFERENCE ADDITIONAL FAB NOTES IN FILE README.TXT

LAYER STACKUP	FILE NAMES
PRIMARY SILKSCREEN	53xx-EB64_PSS.PHO
PRIMARY SOLDERMASK	53xx-EB64_PSM.PHO
PRIMARY SIDE	53xx-EB64_PRL.PHO
370HR - 7MIL THK	
RF ROUTE/GND	53xx-EB64_L02.PHO
370HR - 7MIL THK	
GROUND PLANE	53xx-EB64_L03.PHO
370HR	
DIGITAL ROUTE/GND	53xx-EB64_L04.PHO
370HR	
VDD0x, VDDOUT, GND	53xx-EB64_L05.PHO
370HR	
GROUND PLANE	53xx-EB64_L06.PHO
370HR - 7MIL THK	
RF ROUTE/GND	53xx-EB64_L07.PHO
370HR - 7MIL THK	
SECONDARY SIDE	53xx-EB64_SEC.PHO
SECONDARY SOLDERMASK	53xx-EB64_SSM.PHO
SECONDARY SILKSCREEN	53xx-EB64_SSS.PHO

SCALE: NONE

SIZE	QTY	SYM	PLT	TOOL	TOL
0.006	1379	+	P	1	+0/-0.006
0.012	699	X	P	2	+0/-0.012
0.020	3	□	P	3	+/-0.003
0.040	213	◇	P	4	+/-0.003
0.052	4	⊗	P	5	+/-0.003
0.070	10	⊗	P	6	+/-0.003
0.091	4	A	P	7	+/-0.003
0.125	8	B	P	8	+/-0.003

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DIMENSIONS ARE IN INCHES AND APPLY AFTER FINISH DIMENSIONS IN BRACKETS () ARE IN MILLIMETERS INTERPRET DRAWING PER MIL-D-1000		TOLERANCES		NAME: Si53xx-EB64	
HOLE TOLERANCES PER 78027		PART TO BE FREE OF BURRS		SIZE: B	
DECIMALS XX +/- XXX +/-	ANGLES +/-	SURFACES MICRONS	DESIGN LAYOUT	TT CT	21APR2017 0606C2017
BREAK EDGES		BEND RADIUS	BEND RELIEF	DO NOT SCALE DRAWING	
MAX		MAX	MAX	SCALE: 1:1	
FABRICATION DRAWING				SHEET 1 OF 1	